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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,995	07/28/2003	Arnold M. Frisch	CRED 2618	7355

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,995	FRISCH, ARNOLD M.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *19-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-28 are present for examination and/or are addressed within this action.

Election/Restrictions

Newly submitted claim 1-28 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

I. Claims 1-18 and 26-28, drawn to an apparatus for responding to each edge of an input strobe signal by generating a corresponding edge in each of first and second strobe signals, wherein corresponding in the first and second strobe signals are separated by a target delay, classified in class 714, subclass 700 (skew detection/correction).

II. Claims 19-25, drawn to a built-in self-test (BIST) circuit embedded in an integrated circuit (IC), classified in class 714, subclass 733 (Built-in test circuit (BILBO)).

Inventions [I] and [II] are related as combination and subcombination. Invention in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP 806.05(c)).

In the instant case, the combination (I) as claimed does not require the particulars of the subcombination (II) as claimed because the combination does not require, "a BIST ce[illegible]or producing a state change in the path input signal and for thereafter sampling the pa[illegible]tput signal to determine its state, wherein the state change and the

sampling are separated in time by the target delay and are initiated by corresponding edges in first and second strobe signals also separated in time by the target delay".

The second part of the combination/subcombination requirement is that the subcombination has utility by itself or in other combinations. In the instant case, the subcombination could be used in "A built-in self-test (BIST) circuit embedded in an integrated circuit (IC) for determining whether a state change in a path input signal supplied to an input of a signal path within an integrated circuit (IC) produces a state change in a path output signal appearing at an output of the signal path with a delay exceeding a target delay indicated by input data".

Because the inventions are distinct for the reasons given and have acquired at least two separate classifications in the art, restriction for examination purposes is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-25 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Priority

Examiner inadvertently did not acknowledge the priority date used for this application in the previous action so as to make it of record. Acknowledgement is being made now that no priority either foreign or domestic is claimed for this application and as such the filing date (07/28/2003) is being used for this examination of the elected

claims 1-18 and 26-28 which were elected by the applicant in response to the Election/Restriction mailed to the applicant on 02/24/2006.

Claim Objections

Claims 19-25 are objected to because of the following informalities:

These claims were not elected by the applicant for the office to exam in response to the Election/Restriction mailed to the applicant on 02/24/2006 and as such should not be present in the newly submitted claims by the applicant for the office to examine.

Appropriate correction is required. Examiner notes that this objection to claims 19-25 will only be overcome when applicant has canceled and removed the non-elected claims from the listing of claims submitted to the office for examination. Claims 19-25 will not be given further consideration in this examination since the applicant did not elected these claims for examination.

Claim 26 objected to because of the following informalities:

In line 5 of the submitted claims there is an indention after "the apparatuse comprising:" and before "means for."

Appropriate correction is required. For the purposes of this examination this indent will be treated as an indication that the limitation starting with "means for" in line 5 of the submitted claims is included within "the apparatus" and as such starts on the following line with the claim and includes the indention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 26 recites the limitation "the first circuit" in line 28 on the claim. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination "the first circuit" will be treated as "a first circuit" since there is no prior reference to "a first circuit" being that this is an independent claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1-3, 10-18, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al. (U.S. Patent 6798241 B1) and further in view of Rajski et al. (U.S. Patent 6728901 B1).

1. As per claim 1, Bauer teaches an apparatus (500 – figure 5) for responding to each edge of an input strobe signal (D0 – figure 5) by generating a corresponding edge in each of first and second strove signals (see figure 5 and figures 7A-7E), wherein

corresponding edges in the first and second strobe signals are separated by a target delay referenced by input data (see figures 7C-7E and columns 2-3 illustrating the delay), the apparatus comprising:

A first multiplexer (520 – figure 5) for receiving the input strobe signal and the first and second strobe signals (see figure 5), and for providing any one of the input, first and second strobe signals selected by first selection control data as a first multiplexer output signal (see figure 5);

A control circuit receiving the input data and the first multiplexer output signal for supplying the first selection control data to the first multiplexer and for supplying the delay control data to the first circuit (columns 2-3).

Bauer does not specifically teach:

A first circuit for generating the first and second strobe signals in response to the first multiplexer output signal such that each edge in the first multiplexer output signal subsequently produces a corresponding edge in the first and second strobe signals, with corresponding edges in the first and second strobe signals being separated in time by a programmable delay set by delay control data wherein the generated signals are inputted back to the first multiplexer creating a liner feedback shift register (LFSR).

However in an analogous art Rajski teaches of a linear feedback shift register (LFSR) wherein a multiplexer selects between an input and generated input(s) produced from the output of the multiplexer (see figure 12).

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the LFSR taught within Rajski within Bauer

so that as stated within Bauer the desired timing between generated signals produced by the circuitry can be created within a desired alignment (column 2-3 lines 59-3) in addition to expanding and delaying an input such as stated within Rajski (column 12 lines 6-67).

2. As per claim 2, Bauer in combination with Rajski teaches the apparatus wherein the control circuit carries out a calibration process wherein it sets the delay control data so that the programmable delay between corresponding edges of the first and second strobe signals matches the target delay referenced by the input data (Bauer - columns 2-3).

3. As per claim 3, Bauer in combination with Rajski teaches the apparatus wherein following the calibration process, the control circuit sets the first selection control data so that the first multiplexer provides the input strobe signal as the first multiplexer output signal such that a next edge of the input strobe signal will result in corresponding edges in the first and second strobe signals separated in time by the target delay (Bauer - columns 2-3).

4. As per claim 10, Bauer in combination with Rajski teaches the apparatus wherein the first circuit comprises:

A tapped delay line having N taps for conveying the first multiplexer output signal to each of its N taps in succession, where N is greater than two (Bauer - see figure 5 and column 5 lines 1-2);

A second multiplexer (Bauer - 520 – figure 5) for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a second multiplexer output signal (Bauer - see figure 5); and

First means for generating the first strobe signal in response to the second multiplexer output signal (Bauer - see figure 5).

5. As per claim 11, Bauer in combination with Rajski teaches the apparatus wherein the first circuit further comprises:

Second means for generating the second strobe signal in response to the first multiplexer output signal with a delay substantially matching a delay between an edge of the first multiplexer output signal arriving at any tap selected by the delay control data and a corresponding edge of the first strobe signal generated by the second means (Bauer - see figure 5).

6. As per claim 12, Bauer in combination with Rajski teaches the apparatus wherein the first circuit further comprises:

A third multiplexer for providing the first multiplexer output signal conveyed to any one of the N taps selected by the delay control data as a third multiplexer output signal, wherein the delay control data independently controls the tap selection made by the second and third multiplexer (Bauer - see figure 5 and column 12); and

Second means for generating the second strobe signal in response to the third multiplexer output signal (Bauer - see figure 5).

7. As per claim 13, Bauer in combination with Rajski teaches the apparatus wherein the first circuit provides a first signal path for delaying the first multiplexer output signal

with a first delay to produce the first strobe signal, the first delay being controlled by the delay control data (Bauer - see figure 5),

Wherein the first signal path includes a first number of gates (Bauer - see figure 5),

Wherein the delay control data controls a magnitude of the first number (Bauer - see figure 5 and column 5),

Wherein the first delay is a function of a sum of delays through the first number of gates (see figure 5).

8. As per claim 14, Bauer in combination with Rajski teaches the apparatus wherein a delay through each gate of the first number of gates is a function of the delay of the delay control data (Bauer - see figure 5).

9. As per claim 16, Bauer in combination with Rajski teaches the apparatus wherein the first circuit provides a second signal path for delaying the second multiplexer output signal with a second delay to produce the second strobe signal, the second delay being controlled by the delay control data (Bauer - see figure 5),

Wherein the second signal path includes a second number of gates (Bauer - see figure 5),

Wherein the delay control data controls a magnitude of the second number (Bauer - see figure 5), and

Wherein the second delay is a function of a sum of delays through the second number of gates (Bauer - see figure 5 and column 5).

10. As per claim 17, Bauer in combination with Rajski teaches the apparatus wherein a delay through each gate of the first number of gates is variable and a function of the delay control data (Bauer - columns 4-5 and column 12 lines 45-48), and wherein a delay through each gate of the second number of gates is variable and a function of the delay control data (Bauer - columns 4-5 and column 12 lines 45-48).

11. As per claims 18 and 15, Bauer in combination with Rajski the apparatus wherein the first signal path comprises a first variable capacitor (Bauer - column 5 lines 1-2 and column 12), wherein the delay control data controls a first capacitance of the first variable capacitor (Bauer - column 5 and column 12 lines 45-48), and wherein the first delay is a function of the first capacitance (Bauer - see figure 5), wherein the second signal path comprises a second variable capacitor (Bauer - column 5 lines 1-2 and column 12), wherein the delay control data controls a second capacitance of the second variable capacitor (Bauer - column 5 and column 12 lines 45-48), and wherein the second delay is a function of the second capacitance (Bauer - see figure 5).

12. As per claim 26, Bauer teaches an apparatus for responding to each edge of an input strobe signal (D0 – figure 5) by generating a corresponding edge in each of first and second strobe signals (figures 7A-7E, columns 2-3, and column 5 lines 46-48), wherein corresponding edges in the first and second strobe signals are separated by a target delay referenced by the input data (see figures 7C-7E, figure 5, and columns 2-3), the apparatus comprising:

Means for generating an edge of the first strobe signal in delayed response to each edge of the input strobe signal (see figure 5 and figures 7C-7E);

A first multiplexer (520 – figure 5) for receiving the input strobe signal and the second strobe signal (see figure 5) and for providing either one of the input and second strobe signals selected by the first selection control data as the first multiplexer output signal (see figure 5 and columns 4-5);

A tapped delay line comprising a plurality of gates connected in series for receiving the first multiplexer output signal (see figure 5 and column 5 lines 1-2) and producing an edge in a separate tap signal at an output of each gate in delayed response to each edge in the first multiplexer output signal (see figures 7C-7E and column 4), wherein a signal delay through each gate is a function of voltage supplied to the gates (column 12);

Means for adjusting the voltage supplied to the gates in response to delay control data (column 12 and columns 2-3);

A control circuit receiving the input data and the first multiplexer output signal for supplying the first selection control data to the first multiplexer and for supplying the delay control data to the first circuit, wherein the first selection control data and the delay control data are functions of the input data (columns 2-3).

Bauer does not specifically teacher:

Means for receiving the tap signal produced by each gate as input, for selecting one of the tap signals as a selected tap signal in response to the delay control data and for generating an edge in the second strobe signal in response to each edge in the selected tap signal wherein the generated second strobe signal is inputted back to the first multiplexer creating a liner feedback shift register (LFSR).

However in an analogous art Rajski teaches of a linear feedback shift register (LFSR) wherein a multiplexer selects between an input and generated input(s) produced from the output of the multiplexer (see figure 12).

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the LFSR taught within Rajski within Bauer so that as stated within Bauer the desired timing between generated signals produced by the circuitry can be created within a desired alignment (column 2-3 lines 59-3) in addition to expanding and delaying an input such as stated within Rajski (column 12 lines 6-67).

13. As per claim 27, Bauer in combination with Rajski teaches the apparatus wherein the control circuit carries out a calibration process wherein it sets the delay control data so that a delay between corresponding edges of the first and second control signals match the target delay referenced by the input data (Bauer - column 2-3).

14. As per claim 28, Bauer in combination with Rajski teaches the apparatus wherein the calibration process comprises setting the first selection control data so that the first multiplexer selects the second strobe signal as the first multiplexer output signal and measuring a period of the first multiplexer output signal (Bauer - columns 2-3 and see figure 7C and 13A).

Claim 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al. (US 6798241 B1) and in view of Rajski et al. (U.S. Patent 6728901 B1) as applied to claim 2 above, and further in view of Gillis et al. (6058496).

15. As per claim 4, Bauer teaches the apparatus in accordance with claim 2 as described above in this action.

Bauer does not specifically teach while during the calibration process the control circuit generates count data indicating a difference between first and second quantities, wherein the first quantity is a number of edges of a reference clock signal occurring during a first period determined by counting a predetermined number of edges of the first multiplexer output signal occurring while the first multiplexer providing the first strobe signal as the first multiplexer output signal, and wherein the second quantity is a number of edges of a reference clock signal occurring during a second period determined by counting the predetermined number of edges of the first multiplexer output signal.

However in an analogous art, Gillis teaches measurements (frequency and period) taken from two signals at two distinct times and then obtaining a difference between the two measurements in-order to adjust a programmable delay to a desired delay value (column 7).

Therefore, one would be motivated to combine the teaches of Bauer with Gilles' teachings in instances where it is desired to have signals stepwise separated in time until a desired signal is centered/delayed over an edge of another signal as indicated by Bauer (column 2).

16. As per claims 5 and 7, Gillis teaches the apparatus wherein during the calibration process the control circuit iteratively carries out a process of generating the count data, comparing the count data to the input data, and adjusting the delay control data to

determine a value for the delay control data that sets the programmable delay equal to the target delay (column 7 lines 34-55).

17. As per claim 6, Bauer teaches the apparatus in accordance with claim 4 wherein the control circuit decrements the count data in response to edges of the reference clock signal during the first period and increments the count data in response to edges of the reference clock signal during the second period (column 4).

18. As per claim 8, Bauer teaches the apparatus in accordance with claim 7 wherein following the calibration process, the control circuit sets the first selection control data so that the first multiplexer provides the input strobe signal as the first multiplexer output signal such that a next edge of the input strobe signal will result in corresponding edges in the first and second strobe signals separated in time by the target delay (column 2-3).

19. As per claim 9, the apparatus in accordance with claim 6 wherein the control circuit comprises:

A first counter for counting edges of the first multiplexer output signal and for generating a gate signal indicating when the first and second periods are occurring (Bauer: columns 4-5);

A second counter for decrementing the count data in response to edges of the reference clock signal when the gate signal indicates the first period is occurring and for incrementing the count data in response to edges of the reference clock signal when the gate signal indicates the second period is occurring (Bauer: columns 4-5); and

Means for incrementing or decrementing the delay control data depending on relative magnitudes of the count data and the delay data (Gillis: column 7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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